

Notice of References Cited

Application/Control No.

10/644,730

Applicant(s)/Patent Under
Reexamination
SEKIDO ET AL.

Examiner

Andre Pierre-Louis

Art Unit

2123

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,795,802	09-2004	Yonezawa et al.	703/19
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*	D	US-6,144,931	11-2000	Toda, Takeshi	703/13
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Krabbenborg et al. (IEEE 1996) teaches a Layout to Circuit Extraction for Three-Dimension Thermal-Electrical Circuit Simulation of Device Structures, Pgs.765-774.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.